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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/825,914 | 04/16/2004 | Shigeo Kusunoki | 450100-05023 | 8908 |

7590 05/17/2007

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| EXAMINER | |
|---|---|
| DSOUZA, JOSEPH FRANCIS A | |
| ART UNIT | PAPER NUMBER |
| 2611 | |
| MAIL DATE | DELIVERY MODE |
| 05/17/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/825,914 | KUSUNOKI, SHIGEO | |
| | Examiner | Art Unit | |
| | Adolf DSouza | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 2, 7* is/are rejected.

7)☒ Claim(s) *3 - 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsimbinos et al. (The computational complexity of nonlinear compensators based on the Volterra inverse) in view of Kim (US 20020181611).

Regarding claim1, Tsimbinos discloses a distortion compensation circuit for generating a predistortion signal to perform distortion compensation of a power amplifier (Abstract; wherein the distortion compensation circuit is based on the Volterra inverse) comprising:

subtractor means supplied with the output data of the A/D converter means (page 388, Fig. 7, element subtractor which produces the error signal that is fed to the adaptive Volterra filter);

voltage value data output means for outputting a voltage value data corresponding to the output data of the subtractor means by selecting from a plurality of pieces of previously stored voltage value data (page 388, section 3.1; Fig. 7, element "Adaptive

Volterra Filter"; which receives the subtractor output and produces an output based on the Volterra inverse operators);

amplitude impulse response accumulation adding means for outputting an accumulation adding value of multiplication values obtained by multiplying the signal voltage value after quadrature modulation by impulse response values corresponding to amplitude characteristic of the power amplifier in accordance with the voltage value data from the signal voltage value data outputting means and supplying to the subtractor means (page 388, Figures 3 – 6; section 3.1; wherein the Volterra output is calculated based on Figures 3 – 6, where the amplitude impulse response is interpreted as the Volterra inverse operators and the adding means are the summers shown in Figures 3 - 6);

Tsimbinos does not disclose and ADC, quadrature modulating a baseband signal, and a DAC for converting the predistorted signal to a analog signal.

In the same field of endeavor, however, Kim discloses A/D converter means for digitizing a voltage value of a signal (Fig. 1,element 8) after quadrature modulating a baseband signal (Fig. 1, element 20; paragraph 13, 17);

and D/A converter means for converting the voltage value data from the voltage value data outputting means into an analog signal as an output predistortion signal regarding the amplitude component of the power amplifier (Fig. 1, elements 10, 120; wherein the predistorter is element 120 and the predistorted signal is converted to analog from by the DACs 10).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Kim, in the system of Tsimbinos because this would allow the signals to be digitized, predistorted and modulated, as is well known in the art.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsimbinos et al. (The computational complexity of nonlinear compensators based on the Volterra inverse) in view of Kim (US 20020181611) and further in view of D'Andrea et. al (RF power amplifier Linearization through amplitude and phase predistortion).

Regarding claim 2, Tsimbinos does not disclose a phase impulse response accumulation means.

In the same field of endeavor, however, D'Andrea discloses phase impulse response accumulation adding means for outputting accumulation adding values of converted values obtained by changing code of the impulse response values depending on the voltage value after quadrature modulation and a phase characteristic of said power amplifier in response to the voltage value data from said voltage value data output means; and phase shift means for phase-shifting a phase of the predistortion signal regarding the amplitude component supplied to the power amplifier based on the accumulation adding values from said phase impulse response accumulation adding

means (page 1478, section II; Fig. 2, elements after the $|.|^2$ which does the phase predistortion).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by D'Andrea, in the system of Tsimbinos because this would allow the signals to be phase predistorted, as is disclosed by D'Andrea.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsimbinos et al. (The computational complexity of nonlinear compensators based on the Volterra inverse) in view of Kim (US 20020181611) and further in view of Kerth et. al (US 5,579,247).

Regarding claim 7, Tsimbinos does not disclose up conversion and removal of electromagnetic interference.

In the same field of endeavor, however, Kim discloses a conversion section supplied with the output signal from the distortion compensation section for effecting frequency conversion (Fig. 1, element 20; which up converts the predistorted signal 120 output to RF).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Kim, in the system of

Tsimbinos because this would allow the predistorted signal to be up converted, as disclosed by Kim.

In the same field of endeavor, however, Kerth a removing section for removal of electromagnetic interference (Abstract; column 1, lines 45 – 51; wherein the electromagnetic interference is removed by the filters).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Kerth, in the system of Tsimbinos because this would allow the electromagnetic interference to be removed, as disclosed by Kerth.

### *Allowable Subject Matter*

5. Claims 3 - 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Other Prior Art Cited*

6. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to predistortion of power amplifiers:

Walsh (US 4,835,493) discloses Very wide bandwidth linear amplitude modulation of RF signal by vector summation.

Voyce et al. (US 4,929,906) discloses amplifier linearization using down/up conversion.

Sari (US 4,967,164) discloses an adaptive predistortion circuit.

Cavers (US 5,049,832) discloses amplifier linearization by adaptive predistortion.

Murata (US 5,396,190) discloses Circuit for compensating for nonlinear distortion in transmit power amplifier.

***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER